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EXAMINER
CRAIG, DWIN M

ART UNIT	PAPER NUMBER
2123	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/591,433	IZUMI ET AL.	
	Examiner	Art Unit	
	DWIN M. CRAIG	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/27/2006;12/05/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 have been presented for examination.

Priority

2. The Examiner acknowledges Applicants' claim to foreign priority to PCT/JP05/03728.

Information Disclosure Statement

3. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609.04(a) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

On page 2 of the specification is listed U.S. Pat. 5,859,884 which has not been considered as to the merits.

Specification

4. A substitute specification including the claims is required pursuant to 37 CFR 1.125(a) because the current specification is filled with non-idiomatic English phrases, for example, on page 12 is disclosed,

As described above, implementing the functional unit in the FPGA, which is actual hardware, to test the functional unit allows errors in off-the-shelf software including a synthesis tool and a writing tool in the FPGA to be simultaneously verified.

The sentence is disjoint and contain phraseology that appears to have little or no connection to the beginning of the phrase, for example, the sentence above is saying, *implementing a functional unit in an FPGA allows for verification of the off-the-shelf software and the synthesis tool* and yet the sentence is so disjoint that the Examiner is unable to determine if this interpretation of the sentence is correct.

As another example, on page 5 is the phrase;

In order to prevent the errors due to the timing, it is necessary to design the system allowing for the errors by timing simulation or the like and to apply a general design technique, such as adoption of a synchronous design in which the values are less apt to be indeterminate, to the external interface.

It is unclear from the disjoint sentence what relationship the external interface has to preventing errors.

Merely correcting these two sentences will not fulfill the requirement to correct the specification, a complete editorial review is required for a substitute specification to be entered.

A substitute specification must not contain new matter. The substitute specification must be submitted with markings showing all the changes relative to the immediate prior version of the specification of record. The text of any added subject matter must be shown by underlining the added text. The text of any deleted matter must be shown by strike-through except that double brackets placed before and after the deleted characters may be used to show deletion of five or fewer consecutive characters. The text of any deleted subject matter must be shown by being placed within double brackets if strike-through cannot be easily perceived. An accompanying clean version (without markings) and a statement that the substitute specification

contains no new matter must also be supplied. Numbering the paragraphs of the specification of record is not considered a change that must be shown.

A substitute specification in proper idiomatic English and in compliance with 37 CFR 1.52(a) and (b) is required. The substitute specification filed must be accompanied by a statement that it contains no new matter.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 1-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The claims are generally narrative and indefinite, failing to conform with current U.S. practice. They appear to be a literal translation into English from a foreign document and are replete with grammatical and idiomatic errors.

5.1 More specifically and referring to independent claims 1 and 13 the phrase, the digital logic includes functional units in which logic output patterns correspond to all input logic patterns are verified *in advance*, it is unclear what the *metes and bounds* of the phrase *in advance* is disclosing. It would appear that Applicants' independent claims are teaching a time line of some sort in which there is a period in which the verification is performed and also a period before verification is performed but it is unclear what effect on the scope of the claims is being

provided as to when this verification step is performed. Further claim 1 is a system claim and performing a verification at a specific time fails to further limit a system claim.

Clarification and amendment are required.

Claims 2-12, 14 and 15 have inherited the defects of independent claims 1 and 13, further the Examiner requests that Applicants' review the claim language of all of the claims in the instant case and provide an amended version of said claims that conforms to current U.S. practice.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

6. Claims 1-15 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-24 of U.S. Patent No. 7,512,917. Although the conflicting claims are not identical, they are not patentably distinct from each other because

while the instant case the independent claims teach a safety protection system for a nuclear reactor the claims in 7,512,917 are directed towards a safety apparatus and it would have been obvious, at the time of the invention for an artisan of ordinary skill to have used the claimed safety apparatus of 7,512,917 in a nuclear power safety protection system.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3, 7, 9, 11, 13, 14 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by "Applying Build-In Self-Test to Majority Voting Fault Tolerant Circuits" hereafter referred to as *Stroud et al.*

7.1 As regards independent claims 1 and 13 and using claim 1 as an example, *Stroud et al.* discloses, *a safety protection instrumentation system for a nuclear reactor constructed using digital logic* see page(s) 305 & 306 in the section entitled "Verification and Simulation Results".

wherein digital logic includes functional units (see Figure 2 "Circuit Module 1" Circuit Module 2" etc...) in which output logic patterns correspond to all input logic patterns are verified in advance and a functional module formed by combining the functional units (as regards verification see page(s) 305 & 306 as regards a teaching of output logic patterns and input logic

patterns see the discussion regarding test pattern generators in the portion of *Stroud et al.* entitled "3. BIST for Fault Tolerant Circuits" as regards the teaching so input logic patterns see the sentence in section 3. BIST for Fault Tolerant Circuits "As a result, detecting the presence of single and multiple faults will indicate a need for potential system repairs in the future but, the majority voting fault tolerant circuit must then be tested for its ability to mask these faults and provide the *correct output response for any given input stimuli*." *Emphasis added*).

7.2 As regards claim 2, *Stroud et al.* discloses, wherein each of the functional units individually implements the output logic patterns corresponding to all the input logic patterns on hardware and determines whether the output values coincide with predicted values calculated from design specifications, (see Figure 1 and the discussion regarding test patterns).

7.3 As regards claim 3, *Stroud et al.* discloses, duplicate circuit modules, see the discussion on the page with Figure 2 repeated here… "Given the same initialization values, each *replicated circuit* would ideally be tested with identical sets of test patterns, compacting identical output responses." Replicated circuits will have same gate structure.

7.4 As regards claim 7, *Sroud et al.* discloses, wherein the safety protection instrumentation system is structured so as to generate input patterns in accordance with design specifications of the functional module and to determine whether the output patterns corresponding to the input patterns in the functional module coincide with predicted values calculated from the design specifications. (see the section entitled, "3. BIST for fault tolerant circuits" a portion of which is

repeated here; *These two testing requirements (the ability to detect all multiple stuck-at faults and the ability to verify proper operation in the presence of compensating module faults) have several implications on BIST when applied to fault tolerant circuits as well as on the structure of the fault tolerant circuit. In order to facilitate verification of proper operation in the presence of faults, test pattern generators (TPGs) must be placed at the inputs of the replicated circuit modules while output response analyzers (ORAs) must be placed at the outputs of the MVCs. The TPG placement provides for single and multiple stuck-at fault detection in the replicated circuit modules as well as the MVCs [4] while the ORA placement allows the MVCs to mask compensating module faults. When implementing the fault tolerant circuit, the MVCs should be placed between the outputs of the replicated combinational logic functions and the inputs to the replicated flip-flops. This MVC placement allows the TPG and ORA circuits to be constructed from the flip-flops of the fault tolerant circuit.* The *output response analyzers* will determine whether the output patterns corresponding to the input patterns in the functional module coincide with predicted values calculated from the design specifications.

7.5 As regards claim 9, *Sroud et al.* discloses, wherein the safety protection instrumentation system performs addition or comparison of two variables in the functional unit to replace either one of the two variables with a constant that can be specified with an address having the number of bits smaller than that of the variable, (replacing a variable with a constant is being interpreted to be performing a stuck bit test, see the abstract).

7.6 As regards claim 11, *Sroud et al.* discloses, wherein the functional unit has a function of calculating maximum and minimum output values by a simple expression and a function of passing the maximum and minimum output values, and wherein the safety protection instrumentation system includes a trip evaluator that compares signal values with the maximum and minimum output values to determine whether the signal values are appropriate and an abnormality diagnosis circuit that outputs an abnormal operation signal, See the section entitled, "3. BIST for Fault Tolerant Circuits".

7.7 As regards claim 14, *Stroud et al.* discloses, wherein data processing in the functional units in the safety protection instrumentation system is serially performed in the order of connection, and the serial transmission of a signal is confirmed by monitoring an output timing and it is determined whether the signal is output as designed to verify the performance of the safety protection instrumentation system, see section 1.2 Modified Circular BIST a portion of which is presented here, "The structure is designed to operate either in one Circular BIST chain that incorporates the whole circuit or in R separate, but identical, Circular BIST chains that partition each set of circuit modules and MVCs. Multiplexers sharing a common control input are incorporated between each of the R input and output sections of the Circular BIST chain to configure the chain into the one large chain or R identical chains.", Verifying the structure in R separate, but identical BIST chains is functionally the same as performing the verification in a serial manner.

7.8 As regards claim 15 *Stroud et al.* teaches, comprising the step of verifying whether the functional units in the safety protection instrumentation system have same structure as an internal structure when performance of the functional units is verified, See the section entitled, "3. BIST for fault tolerant circuits".

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Stroud et al.* in view of U.S. Patent 6,587,979 to *Kraus et al.*

8.1 As regards claim 4, *Stroud et al.* does not expressly disclose, wherein the functional module formed by combination of the functional units includes a register thorough which an output from the functional unit is transmitted and a delay element used for adjusting the timing of signal processing in the functional unit.

However, *Kraus et al.* teaches a programmable delay to assist in circuit testing, see "A skew circuit 81 adjustably delays each of the DI, ADDR and CNT outputs of data generator 60, filters 78 and 80, and sequencer 72 with delays controlled by the SKEW data input from JTAG register 55 of FIG. 6. The delays are set to accommodate the timing requirements of the RAM under test.", in Col. 16 lines 29-34.

Stroud et al. and *Kraus et al.* are analogous art because they both come from the same problem solving area of circuit testing and verification.

At the time of the invention, it would have been obvious to an artisan of ordinary skill to have used the delay methods of *Kraus et al.* to verify the safety protection circuits of *Stroud et al.*

The motivation for doing so would have been, to provide a build-in test circuit in an embedded system to test circuits without having to provide a custom BIST after the design has

been complete and to therefore make verification of circuits easier, see Col. 2 lines 32-56 of *Kraus et al.*

Therefore, it would have been obvious to combine the teachings of *Kraus et al.* with the teachings of *Stroud et al.* to obtain the invention as specified in the claim 4.

9. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Stroud et al.* in view of U.S. Patent 5,805,608 to Baeg et al.

Stroud et al. doesn't expressly disclose, wherein the functional module formed by combination of the functional units includes a register thorough which an output from the functional unit is transmitted and uses handshaking for transferring a signal between the functional unit that drives the register at different clock frequencies, among the functional units.

However, *Baeg et al.* teaches a programmable clock used for BIST testing in logic circuits see Figure(s) 2F and 4 and Col. 2 lines 64-67 and Col. 3 lines 1-67 and Col. 4 lines 1-3 more specifically "in some manufacturing tests, clocks psca, pscb are non-overlapping clocks having equal frequencies", which clearly infers that in other configurations there are clocks of different frequencies, see also Table 1, as regards a teaching of handshaking see the descriptive text.

Stroud et al. and *Baeg et al.* are analogous art because they both come from the same problem solving area of circuit testing and verification.

It would have been obvious, at the time of the invention, to an artisan of ordinary skill to have used the clock frequency teachings of *Baeg et al.* with the safety circuit verification teachings of *Stroud et al.*

The motivation for doing so would have been because it is desirable to provide simple clock generation circuitry, see *Baeg et al.* Col. 1 lines 15-42.

Therefore it would have been obvious to combine the teachings of *Baeg et al.* with the teachings of *Stroud et al.* in order to obtain the invention as specified in the claim 5.

10. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Stroud et al.* in view of U.S. Patent 6,691,079 to Lai et al.

Stroud et al. does not expressly disclose, wherein the safety protection instrumentation system includes software in which effective programs statements executed by hardware and input pattern groups indicating operation paths are described, uses branch coverage or toggle coverage used for evaluating the ratio of the input logic patterns or determining whether the number of the input patterns is sufficient, and determines whether the output logic patterns corresponding to the input logic patterns coincide with predicted patterns calculated from design specifications to verify the connection between the functional units.

However, *Lai et al.* teaches, branch coverage and toggle coverage, see Col. 5 lines 59-67 and Col. 6 lines 1-15.

Stroud et al. and *Lai et al.* are analogous art because they both come from the same problem solving area of digital circuit verification.

At the time of the invention, it would have been obvious to a person of ordinary skill in the logic verification art to have used branch coverage and toggle coverage when performing verification of a logic circuit.

The motivation for doing so would have been to provide a method of performing test coverage on a logic circuit design in less time and therefore perform the tests with greater efficiency, see Col. 1 lines 50-54 of *Lai et al.*

Therefore it would have been obvious to use the test coverage teachings of *Lai et al.* with the logic circuit verification teachings of *Stroud et al.* in order to obtain the invention as specified in claim 6.

11. Claims 8 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Stroud et al.* in view of U.S. Patent 5,621,776 to Gaubatz.

11.1 As regards claim 8, *Stroud et al.* does not expressly disclose, wherein the safety protection instrumentation system includes an analog-to-digital element that converts an analog signal pattern in accordance with design specifications of the functional module into a digital value to generate a digital input pattern and a digital-to-analog element that converts an output corresponding to an input in the functional module into an analog value, and determines whether the analog value coincides with a predicted value calculated from the design specifications.

However, *Gaubatz* teaches analog signals being used in Fault-Tolerant Reactor Protection Systems, see Col. 8 lines 54-67 and Col. 9 lines 1-40.

Stroud et al. and *Gaubatz* are analogous art because they both come from the same problem solving area of Nuclear reactor protection systems.

At the time of the invention, it would have been obvious to a person of ordinary skill to have provided for analog signals in a reactor fault tolerant protection logic circuit.

The suggestion for doing so is provided in *Gaubatz* in Col. 2 lines 25-33 which provides the requirements for a reliable reactor protection system and using analog signals in a test of a fault tolerant logic system fro use in nuclear reactors would be required in order to test the entire system.

Therefore, it would have been obvious to use the teachings of *Gaubatz* with the teachings of *Stroud et al.* in order to obtain the invention as specified in claims 8 and 12.

11.2 As regards claim 12, *Stroud et al.* does not expressly disclose, wherein the safety protection instrumentation system includes a first safety protection instrumentation system that converts a digital output into an analog value and converts the analog value into an optical signal and a second safety protection instrumentation system that converts the optical signal into an analog value and converts the analog value into a digital value, and wherein the first safety protection instrumentation system is connected to the second safety protection instrumentation system.

However, *Gaubatz* teaches, an analog to digital converter, see Col. 7 lines 7-10 and an optical signal, see Col. 7 lines 44-65.

12. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over *Stroud et al.* in view of U.S. Patent 4,517,154 to Dennis et al.

12.1 As regards claim 10, *Stroud et al.* teaches, and wherein the safety protection instrumentation system includes a trip evaluator (see section 4. Verification and Simulation results) however, *Stroud et al.* does not expressly disclose, wherein the functional unit has a

function of passing an operation flag indicating normal completion of the operation, wherein the functional module has a function of monitoring the operation flag, and wherein the safety protection instrumentation system includes a trip evaluator that receives an output from the functional module and determines whether the operation flag is set and an abnormality diagnosis circuit that outputs an abnormal operation signal if the operation flag is not set.

However, *Dennis et al.* teaches flags see Figure 14A, item 101 and item 112 and Col. 11 lines 42-50, more specifically, "analog trip module" which describe setting flags when the reactor safety protection software is executed, see also Col. 12 lines 19-60.

Stroud et al. and *Dennis et al.* are analogous art because they both come from the same problem solving area of reactor safety protection systems.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to have used the flag teachings of *Dennis et al.* with the logic verification teachings of *Stroud et al.*

The motivation for doing so would have been to provide a means by which the nuclear power plants safety protection circuits could be verified and testing without effecting the plants ability to be operated and have faults detected during the verification, see Col. 3 and Col. 4 of *Dennis et al.*

Therefore, it would have been obvious to modify the teachings of *Dennis et al.* with the teachings of *Stroud et al.* in order to obtain the invention as specified in claim 10.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DWIN M. CRAIG whose telephone number is (571)272-3710. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Dwin M Craig/
Examiner, Art Unit 2123